REMARKS

Prior to the present amendment, claims 18-22, 24-25, 27-30, and 32-37 were pending in the present application. By the present amendment, claims 18, 22, 25, 30, 32, and 33 have been amended and claims 19, 21, 27, and 29 have been canceled. Thus, claims 18, 20, 22, 24-25, 28, 30, and 32-37 remain in the present application. Reconsideration and allowance of pending claims 18, 20, 22, 24-25, 28, 30, and 32-37 in view of the above amendments and the following remarks are requested.

A. Rejection of Claims 33-37 under 35 USC §102(b)

The Examiner has rejected claims 33-37 under 35 USC §102(b) as being anticipated by U.S. patent number 5,734,703 to Yuichiro Hiyoshi (hereinafter "Hiyoshi"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claim 33, is patentably distinguishable over Hiyoshi.

The present invention, as defined by amended independent claim 33, includes, among other things, a modem interface circuit including a DC loop current circuit having a first operational amplifier driving a first base of a first electronic inductor transistor and an AC current circuit having a second operational amplifier driving a second base of a second electronic inductor transistor, "wherein a first collector of said first electronic inductor transistor is connected to a second collector of said second electronic inductor transistor." As disclosed in the present application, in one embodiment of the invention a

first operational amplifier/ first transistor combination is used to set DC loop current and a second operational amplifier/second transistor combination is used to drive an AC signal, where the collectors of the first and second transistors are connected to a rectified Tip and Ring voltage.

As disclosed in the present application, the first transistor controls the DC line current, while the second transistor controls the AC line current. As a result of the above configuration, the first transistor can be biased in a non-linear region at any current without introducing distortion on the AC signal, while the second transistor can be biased with a sufficiently low current to operate in a linear region and provide excellent linearity in the AC signal transmitted to the line. Also, as disclosed in the present application, the above configuration advantageously allows the respective gains of the first and second transistors to be set independently for DC and AC.

In contrast to the present invention as defined by amended independent claim 33, Hiyoshi does not teach, disclose, or suggest a modem interface circuit including a DC loop current circuit having a first operational amplifier driving a first base of a first electronic inductor transistor and an AC current circuit having a second operational amplifier driving a second base of a second electronic inductor transistor, "wherein a first collector of said first electronic inductor transistor is connected to a second collector of said second electronic inductor transistor." Hiyoshi specifically discloses circuit driver 520 and semiconductor circuit 540, which are coupled across diode bridge 103. See, for example, Figure 9 and related text of Hiyoshi.

In Hiyoshi, circuit driver 520 includes a transistor driven by an operational amplifier, where the collector of the transistor in circuit driver 520 is coupled to a positive terminal of diode bridge 103. See, for example, Figure 9 of Hiyoshi. In Hiyoshi, semiconductor circuit 540 also includes a transistor driven by an operational amplifier. However, the collector of the transistor in semiconductor circuit 540 is coupled to a negative terminal of diode bridge 103. See, for example, Figure 9 of Hiyoshi. Thus, in Hiyoshi, the collectors of respective transistors in circuit driver 520 and semiconductor circuit 540 are not connected together. However, Hiyoshi fails to teach, disclose, or remotely suggest a modem interface circuit including a DC loop current circuit having a first operational amplifier driving a first base of a first electronic inductor transistor and an AC current circuit having a second operational amplifier driving a second base of a second electronic inductor transistor, where a first collector of the first electronic inductor transistor is connected to a second collector of the second electronic inductor transistor, as specified in amended independent claim 33.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by amended independent claim 33, is not taught, disclosed, or suggested by Hiyoshi. Thus, amended independent claim 33 is patentably distinguishable over Hiyoshi. As such, claims 34-37 depending from amended independent claim 33 are, *a fortiori*, also patentably distinguishable over Hiyoshi for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. **Rejection of Claims 18-22, 24-25, 27-30, and 32 under 35 USC §103(a)**

The Examiner has rejected claims 18-22, 24-25, 27-30, and 32 under 35 USC §103(a) as being unpatentable over Hiyoshi in view of U.S. patent number 4,796,295 to Gay et al. (hereinafter "Gay"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 18 and 25, is patentably distinguishable over Hiyoshi and Gay, either singly or in combination thereof.

The present invention, as defined by amended independent claims 18 and 25, includes, among other things, an electronic inductor transistor driven by an operational amplifier and having a collector connected to a base of a second transistor, "wherein a negative input of said operational amplifier is connected to an emitter of said electronic inductor transistor," and "an impedance matching circuit connected between said positive input of said operational amplifier and a collector of said second transistor." As disclosed in the present application, according to various embodiments of the invention, an electronic inductor transistor and an operational amplifier combine to form a voltage-controlled current source (VCCS) with respect to loop current, where the operational amplifier drives the base of the electronic inductor transistor and receives negative feedback from the emitter of the electronic inductor transistor.

As disclosed in the present application, according to one embodiment of the invention, a second transistor is utilized to provide increased isolation for a modem when the modem is on-hook, where the base of the second transistor is connected to the

collector of the electronic inductor transistor, the emitter of the second transistor is connected to a rectified Tip and Ring voltage, and the collector of the second transistor is connected to a positive input of the operational amplifier via an impedance matching circuit. In the configuration discussed above, the operational amplifier linearizes the voltage signal at the emitter of the electronic inductor transistor (through the negative feedback input), and causes the line current to swing linearly according to the expression I = Ve/Re, where "I" is the line current, "Ve" is the emitter voltage, and "Re" is the value of the emitter resistor.

As disclosed in the present application, by setting the collector voltage well above Ve (the emitter voltage), the present invention advantageously provides an acceptable level of distortion for high-speed modem applications. For example, the present invention can advantageously provide a transmitted signal having harmonic content or distortion that is at least 80 dB below the fundamental signal level.

In contrast to the present invention as defined by amended independent claims 18 and 25, Hiyoshi does not teach, disclose, or suggest an electronic inductor transistor driven by an operational amplifier and having a collector connected to a base of a second transistor, "wherein a negative input of said operational amplifier is connected to an emitter of said electronic inductor transistor," and "an impedance matching circuit connected between said positive input of said operational amplifier and a collector of said second transistor." Hiyoshi specifically discloses a circuit arrangement including semiconductor inductor circuit 540, which is connected across diode bridge 103. See, for

example, Figure 9 and related text of Hiyoshi. In Hiyoshi, semiconductor inductor circuit 540 includes a single transistor driven by an operational amplifier, where the collector of the transistor is connected to a negative terminal of diode bridge 103 and the emitter of the transistor is connected to a positive terminal of diode bridge 103 via a resistor and a zener diode. See, for example, Figure 9 of Hiyoshi.

However, Hiyoshi fails to teach, disclose, or remotely suggest an electronic inductor transistor driven by an operational amplifier and having a collector connected to a base of a second transistor, where a negative input of the operational amplifier is connected to an emitter of the electronic inductor transistor, and an impedance matching circuit connected between a positive input of the operational amplifier and a collector of the second transistor, as specified in amended independent claims 18 and 25.

In contrast to the present invention as defined by amended independent claims 18 and 25, Gay does not teach, disclose, or suggest an electronic inductor transistor driven by an operational amplifier and having a collector connected to a base of a second transistor, "wherein a negative input of said operational amplifier is connected to an emitter of said electronic inductor transistor," and "an impedance matching circuit connected between said positive input of said operational amplifier and a collector of said second transistor." Gay specifically discloses a circuit including high voltage transistors 5 and 6 and operational amplifier 14, where the emitter of high voltage transistor 5 is connected to input terminal 1 of a telephone circuit, the collector of high voltage transistor 5 is coupled via resistor 7 to reservoir capacitor 8 and shunt regulator means 9, the base of high

voltage transistor 5 is connected to the collector of high voltage transistor 6, the base of high voltage transistor 6 is driven by operational amplifier 14, and the emitter of high voltage transistor 6 is connected to ground. See, for example, column 3, lines 6-22 and Figure 1 of Gay.

Applicants note that in Figure 1 of Gay, the collector of high voltage transistor 5 is connected to input terminal 1, while in detailed description section of Gay the emitter of high voltage transistor 5 is connected to input terminal 1. Applicants have assumed that the orientation of high voltage transistor 5 as disclosed in the detailed description section of Gay is the correct orientation. In Gay, the negative input of operational amplifier 14 is coupled to the collector of high voltage transistor 5 via generator 12. See, for example, Figure 1 and related text of Gay. However, Gay fails to teach, disclose, or remotely suggest a negative input of an operational amplifier connected to an emitter of a electronic inductor transistor, as specified in amended independent claims 18 and 25.

Also, in Gay, impedance network 10 is coupled between the emitter of high voltage transistor 5 and a positive input of operational amplifier 18 and impedance network 11 is coupled between the emitter of high voltage transistor 5 and a negative input of operational amplifier 21. See, for example, Figure 1 and related text of Gay. However, Gay fails to teach, disclose, or suggest an impedance matching circuit connected between a positive input of an operational amplifier and a collector of a second transistor, as specified in amended independent claims 18 and 25. Thus, Gay fails to cure the basic deficiencies of Hiyoshi discussed above. Thus, Applicants respectfully submit

that the combination of Hiyoshi and Gay does not and cannot result in the invention as specified in amended independent claims 18 and 25.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by amended independent claims 18 and 25, is not taught, disclosed, or suggested by Hiyoshi and Gay, either singly or in combination thereof. Thus, amended independent claims 18 and 25 are patentably distinguishable over Hiyoshi and Gay. As such, claims 21-22 and 24 depending from amended independent claim 18 and claims 28, 30, and 32 depending from amended independent claim 25 are, *a fortiori*, also patentably distinguishable over Hiyoshi and Gay for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 18, 25, and 33, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 18, 20, 22, 24-25, 28, 30, and 32-37 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 18, 20, 22, 24-25, 28, 30, and 32-37 pending in the present application is respectfully requested.

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Respectfully Submitted,
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